

2155



Please type a plus sign (+) inside this box

PTO/SB/21 (12/97)
Approved for use through 9/30/2000. OMB 0651-0031
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

+

TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	09/851,181	
	Filing Date	May-08, 2001	
	First Named Inventor	Theodore Vaida	
	Group Art Unit	2155	
	Examiner Name		
Total number of pages in this submission	4	Attorney Docket Number	LSIL-01-035 / 01-035

RECEIVED

APR 29 2004

Technology Center 2100

ENCLOSURES (check all that apply)

<input type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Fee Attached <input type="checkbox"/> Amendment/Response <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits(s)/declaration(s) <input type="checkbox"/> Extension of time reques <input type="checkbox"/> Express Abandonment Reques <input checked="" type="checkbox"/> Information Disclosure Statemen <input type="checkbox"/> Certified Copy of Priority Document(s) <input type="checkbox"/> Response to Missing Parts/Incomplete Application <input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53	<input type="checkbox"/> Assignment Papers <input type="checkbox"/> Drawing(s) <input type="checkbox"/> Licensing-related Paper <input type="checkbox"/> Petition Routing Slip (PTO/SB/69) and Accompanying Petition <input type="checkbox"/> To Convert a Provisional Application <input type="checkbox"/> Power of Attorney, Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Small Entity Statement <input type="checkbox"/> Request for Refund	<input type="checkbox"/> After Allowance Communication to Group <input type="checkbox"/> Appeal Communication to Board of Appeals and <input type="checkbox"/> Appeal Communication to Group (Appeal Notice, Brief, Reply Brief) <input type="checkbox"/> Proprietary Information <input type="checkbox"/> Status Letter <input checked="" type="checkbox"/> Additional Enclosure(s) (please identify below): <div style="border: 1px solid black; padding: 5px;"> <p>1. Return address postcard for PTO mailroom to date stamp.</p> </div>
Remarks: 15 references		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Individual Name	Leo Peters, Reg. No. 33,562, Phone: [+1] 408-433-7191
Signature	<i>[Signature]</i>
Date	4/21/04

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope to: Assistant Commissioner for Patents, Washington, D.C. 20231 on this date: 4/21/04	
Typed or printed name	Connie Del Castillo, Phone: [+1] 408-433-7191
Signature	<i>[Signature]</i> Date 4/21/04

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO : Assistant Commissioner for Patents, Washington, DC 20231.

C

#3
LH

A circular black ink stamp from the U.S. Patent & Trademark Office. The text "U.S. PATENT & TRADEMARK OFFICE" is curved along the top and sides of the circle. In the center, the date "APR 26 2004" is stamped. The stamp is partially overlapping the "et al." text on the left and the "Specific Information" text on the right.

~~~~~

5-5-54

**Examiner :**

**Atty Docket :** LSIL-01-035 / 01-035

Connie Del Castillo

4/21/04 Date

Connie Del Castillo  
Connie del Castillo Signature

## RECEIVED

Commissioner for Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

Technology Center 2100

The references listed in the attached form, copies of which are attached, may be material to examination of above-identified application. Applicants submit these references in compliance with their duty of disclosure pursuant to 37 CFR 1.56 and 1.97.

It is requested that the information disclosed herein be made of record in the application.

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that these references indeed constitute prior art.

If it is determined that any additional fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 12-2252.

LSI Logic Corporation  
1551 McCarthy Blvd., MS D-106  
Milipitas, CA 95035  
408-433-7475

Date: 4/21/04

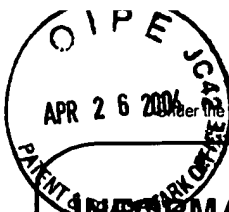
Respectfully submitted,



Leo Peters

Reg. No. 33,562





# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Complete if Known

|                      |                      |
|----------------------|----------------------|
| Applicati n Number   | 09/851,181           |
| Filing Date          | May-08, 2001         |
| First Named Invent r | Theod re Vaida       |
| Group Art Unit       | 2155                 |
| Examiner Name        |                      |
| Attorney Docket No.  | LSIL-01-035 / 01-035 |

# 3

Sheet 1 of 2

RECEIVED

APR 29 2004

Technology Center 2100

## OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

| Examiner Initials | Cite No. | Include name of author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, caalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where | T |
|-------------------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|
|                   |          | A C Compiler for a Processor with a Reconfigurable Functional Unit; Proceedings of the 37th ACM/IEEE Conference on Design Automation Conference, 2000 - Author(s) - YE et al.                                                                   |   |
|                   |          | Using General-Purpose Programming Languages for FPGA Design; DAC 2000 - Author(s) - Hutchings et al.                                                                                                                                            |   |
|                   |          | Reconfigurable Computing: Its Concept and a Practical Embodiment Using Newly Developed Dynamically Reconfigurable Logic (DRL) LSI; ASP-DAC 2000 - Author(s) - Masakazu Yamashina                                                                |   |
|                   |          | Reconfigurable Computing: What, Why and Implications for Design Automation; DAC 1999 - Author(s) - DeHorn et al.                                                                                                                                |   |
|                   |          | An Automated Temporal Partitioning and Loop Fission Approach for FPGA Based Reconfigurable Synthesis of DSP Applications; DAC 1999 - Author(s) - Meenakshi Kaul                                                                                 |   |
|                   |          | Dynamically Reconfigurable Architecture for Image Processor Applications; DAC 1999 - Author(s) - Alexandro Adario                                                                                                                               |   |
|                   |          | A Representation for Dynamic Graphs in Reconfigurable Hardware and its Application to Fundamental Graph Algorithms; FPGA 2000 - Author(s) - Lorenz Huelsbergen                                                                                  |   |
|                   |          | A Reconfigurable Multi-Function Computing Cache Architecture; DCNL Conference 2000 - Author(s) - Kim et al.                                                                                                                                     |   |
|                   |          | Communicating Logic: An Alternative Embedded Stream Processing Paradigm; ASP-DAC 2000 - Author(s) - Imlig et al.                                                                                                                                |   |
|                   |          | The Application of Genetic Algorithms to the design of Reconfigurable Reasoning VLSI Chips; FPGA 2000 - Author(s) - Moritoshi Yasunaga                                                                                                          |   |
|                   |          | A Benchmark Suite for Evaluating Configurable Computing Systems - Status, Reflections, and Future Directions; FPGA 2000 - Author(s) - Kumar et al.                                                                                              |   |
|                   |          | A Scheduling and Allocation Method to Reduce Data Transfer Time by Dynamic Reconfiguration; Asia and South Pacific DAC 2000 - Author(s) - Kazuhito Ito                                                                                          |   |
|                   |          | An Architecture-Driven Metric for Simultaneous Placement and Global Routing for FPGA's ; DAC 2000 - Author(s) - Chang et al.                                                                                                                    |   |

|                    |  |                |  |
|--------------------|--|----------------|--|
| Examin r signature |  | Dat c nsider d |  |
|--------------------|--|----------------|--|



OIPE JC  
 APR 26 2004  
 PATENT & TRADEMARK OFFICE



# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Complete If Known

|                      |                      |
|----------------------|----------------------|
| Applicati n Numb r   | 09/851,181           |
| Filing Date          | May-08, 2001         |
| First Named Inv nt r | The d r Valda        |
| Group Art Unit       | 2155                 |
| Examiner Name        |                      |
| Attorney Docket No.  | LSIL-01-035 / 01-035 |

|       |   |    |   |
|-------|---|----|---|
| Sheet | 2 | of | 2 |
|-------|---|----|---|

|  |                                                                                                                                                                                                                       |  |
|--|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|
|  | MorphoSys: Case Study of a Reconfigurable Computing System Targeting Multimedia Applications; DAC 2000 - Author(s) - Singh et al.                                                                                     |  |
|  | LSI Logic ASICs To Add Programmable-Logic Cores; <a href="http://www.eetimes.com/story/OEG19990729S0001">http://www.eetimes.com/story/OEG19990729S0001</a> ; EE Times; July 29, 1999; 2 pages - Author(s) - MATSUMOTO |  |

RECEIVED

APR 29 2004

Technology Center 2100

|                      |  |                   |  |
|----------------------|--|-------------------|--|
| Examiner<br>signatur |  | Dat<br>consid r d |  |
|----------------------|--|-------------------|--|